In the Drawings:

New Figure 4B is attached. Please replace Figure 4B with the new Figure 4B. The following changes were made to Figure 4B to bring Figure 4B in agreement with the specification:

1). Label **60** was replaced with label **54**.

2). Label **64** within the diode B was replaced with label **68**.

A red-lined copy of new Figure 4B is provided to illustrate the changes that were made.

REMARKS

Amendment to the Specification and Replacement of Figure 4B

Two labels were changed in Figure 4B to bring the new Figure 4B in agreement with the specification. Specifically, label **60** was replaced with label **54**, and label **64** in the diode B was replaced with the label **68**.

Paragraph [0041] was amended to clarify that electrode **68** is in *electrical* contact with the pixel electrode **38**.

The Pending Claims and Amendments

Claims 38-67 and 70-94 were pending prior to this response. By this amendment, claims 49-50 have been cancelled. Therefore, the currently pending claims are 38-48, 51-67 and 70-94.

The Examiner has withdrawn claims 42, 43, 45-48, 50, 61-63, 71, 74, 75, 78, 82-84 and 88-90 following Applicant's response to an election of species requirement. Applicant acknowledges withdrawal of these claims. However, as Applicant has pointed out in his response dated July 1, 2006, the claims readable on elected species include claims 38-42, 44-45, 49-67, 70, 72-74, 76-77, 79-81, 85-87, and 91-94. Therefore Applicant believes that claims 42, 45, 50, 61-63, and 74 have been withdrawn in error and should be re-joined to the claims that are currently under consideration. For example, claim 42 recites that the organic semiconductor includes MEH-PPV. This claim is clearly readable on both elected species IA, and IIA, since MEH-PPV is a species within a genus of organic semiconductors (IA), and within a genus of semiconductor polymers including phenylene units (IIA).

Independent claims 38, 57, and 58 have been amended. Independent claim 38 has been amended to recite that "depositing a semiconductor from solution comprises forming a patterned layer of the semiconductor". Independent claim 57 was amended to recite an operation of "forming a patterned organic semiconductor layer, wherein the organic semiconductor layer overlies at least a portion of the first electrode". Independent claim 58 was amended to recite "forming a patterned semiconductor layer over at least a portion of the first electrode". Support for these amendments is found at paragraph [0027] and in the figures, particularly Figure 3B, and Figures 5C and 5D. Independent claims 38, 57, and 58 have also been amended to focus on a method of forming an active matrix display, the method "comprising obtaining a substrate for use in a backplane of the display". Support for this amendment is found, for example, in paragraphs [0006], [0007], and [0027]. Dependent claims 59, 67, and 72 have been amended to correct typographical errors.

In the Office Action, all claims were rejected. Claims 38-41, 44, 49, 54, 57, 70, 72-73, 76 and 80 were rejected as obvious over a US Patent No. 7,030,412 issued to Drzaic et al. in view of US Patent No. 6,852,555 issued to Roman et al. Other claims were rejected as obvious over Drzaic in view of Roman and further in view of at least one of the following references: US Patent No. 6,087,196 issued to Sturm et al., US Patent No. 6,623,903 issued to Lamotte et al.; US Patent Application Pub. No. 2002/0027636 by Yamada et al., and US Patent Application Pub. No. 2002/0127821 by Ohya et al.

Applicant respectfully traverses all rejections in view of the amendments and remarks presented herein.

103(a) Rejections based on Drzaic and Roman

Independent claim 38 and its dependent claims 39-41, 44, 49, 54, 70, 76, 77, 79, and 94

The Examiner rejected independent claim 38 as obvious over Drzaic in view of Roman. The Examiner points to column 3, line 40, column 11 lines 1-3, and to a not well-specified paragraph of the Drzaic reference as teaching a display comprising thin film diodes with organic semiconductors. The Applicant respectfully disagrees with this assessment of the Drzaic reference. The Drazic reference makes only passing reference to diodes and provides no hint of a diode structure, fabrication method, or composition.

The Drzaic reference describes displays using thin film transistors (TFTs), which are not two-terminal switching devices. The structure of transistors is described in some detail, and the transistors, as described in Drzaic, indeed may include layers of organic material. However, with regard to diodes (two-terminal switching devices), Drzaic provides no detail as to their structure. The diodes are mentioned only once, with one line reciting that "*alternatively non-linear devices can be diodes*" (col. 11, lines 3). Drzaic reference does not make it clear what type of diodes can be used or whether the diodes use organic material layers. For example, there is no teaching or suggestion that they are conductor-semiconductor-conductor devices (MIMs) as recited in the claims. Further, throughout the document, an organic material is never mentioned in conjunction with diodes. Even if Drazic would suggest to one of skill that a diode could be substituted for a transistor in certain applications, Drazic provides no suggestion as to the structure or fabrication method of such diode. Drazic's transistor components have various compositions. For example, they employ inorganic and organic semiconductors (see column 3, lines 65-67 and column 3, lines 63-65). With Drazic's brief mention of diodes, one of skill is not directed to a two-terminal device fabrication method containing the specific arrangement of claimed operations.

As it is well known to those of skill in the art, diodes and transistors are very different electronic devices, having different requirements for their components. One cannot extrapolate that if one material works well in a transistor, it will necessarily work well in a diode. For example, a typical vertical configuration of thin film diodes requires that the layer between the diode electrodes remains pinhole-free, to prevent shorting between electrodes. Since transistors have a different structure, this requirement would not apply in a case of transistor. Therefore, when use of particular materials is disclosed for transistors, it does not automatically become obvious that this material should be used in a diode or in another two-terminal switching device. A more detailed discussion of fundamental differences between transistors and diodes was laid out by the Applicant in Amendment A (page 13, last paragraph and page 14, first and second paragraphs), which was filed in response to Office Action dated September 21, 2005.

The Roman patent does describe a diode structure in some detail, but it is for a wholly different application than backplane or pixel control circuits. Roman does not direct one skilled in the art to use the described diodes in display applications, since it does not teach use of the diodes in displays and is primarily focused on fabrication of memory devices. Further, Roman does not teach patterning a semiconductor layer. Again, because of the fundamental differences between diode and transistor functions, structure, and fabrication methods, one of skill in the art would not be motivated to blindly substitute diodes having the structure and fabrication method of Roman for the transistors described by Drazic.

Further, neither the Drazic patent nor the Roman patent suggest to one of skill in the art that a semiconductor layer should be patterned during fabrication – as recited in independent claims 38, 57, and 58 as amended.

Drzaic mentions that the costs of manufacturing of active matrix displays can be substantially reduced when an unpatterned semiconductor layer spanning several transistors is used (e.g., col. 4, lines 19-26). Such reduction in costs comes at a price of increased cross-talk between the switching elements, which is considered tolerable for some display application. Drzaic does not envision any other way of reducing the display manufacturing costs, and generally teaches away from such patterning.

Contrary to Drzaic's teachings, embodiments recited in an amended claim 38 reduce the costs of fabrication by depositing the semiconductor layer of a two-terminal switching device from solution, "wherein depositing comprises forming a patterned layer of semiconductor material." The recited deposition is a simple pattern-forming operation (performed, e.g., by printing or by other type of selective deposition), which is fundamentally different from previously employed costly vacuum-based deposition methods requiring subsequent photolithographic patterning.

While Examiner points out that "Drzaic discloses that the semiconductor layer can be patterned to reduce crosstalk", the Applicant respectfully submits that Drzaic teaches away from such patterning. In column 1, lines 57-63 Drzaic teaches that "the high cost in manufacturing thin-film transistors results in part from the patterning steps, which require the use of expensive masks in photolithographic setups, and etching steps". Further, in column 2, lines 3-14 Drzaic discloses that "In one aspect, the invention features electronic circuits that have a lower manufacturing cost... In a preferred embodiment, the semiconductor layer is unpatterned." Drzaic does not provide any motivation to form a patterned semiconductor layer during deposition of such layer.

The Roman reference cited by the Examiner fails to overcome this deficiency of Drzaic. The Roman reference is concerned with fabrication of thin film diodes having a two-layer anode, which are used primarily in memory applications. While the Roman reference describes patterning of the electrodes, it does not describe patterning of the semiconductor layer residing between the two electrodes. Roman's semiconductor layer is deposited by spin on coating. Further, the prior art does not provide sufficient motivation to combine Roman with Drzaic, since Roman does not envision display applications, particularly pixel control circuits. Further, even if there was legally sufficient motivation to combine these references, together they fail to teach depositing a patterned semiconductor layer in a two-terminal device.

For at least these reasons, the Applicant respectfully submits that amended independent claim 38 and its dependent claims 39-41, 44, 49, 54, 70, 76, 77, 79, and 94 are not obvious over Drzaic in view of Roman and request withdrawal of a 103 rejection for those claims.

Independent claim 57 and its dependent claims 72, 73, 80, 81, 85, and 93.

Amended independent claim 57 recites that forming a two terminal switching device comprises "forming a patterned organic semiconductor layer". The Applicants submit that use organic semiconductor in such device advantageously results in reduced manufacturing costs, since high-cost vacuum-based deposition methods are typically not required for deposition of organic semiconductors. Patterning of such a layer either during or after the deposition will lead to an array of devices with low cross-talk and with low manufacturing costs.

As it was discussed above, Drzaic does not describe the structure or fabrication of two-terminal switching devices and generally teaches away from patterning. Roman does not teach that his devices can be used in displays or that it is advantageous to pattern the semiconductor layer residing between the two electrodes. Taken together, these two references would not make an invention claimed in claim 57 obvious to one skilled in the art. At least for these reasons, the Applicant respectfully requests withdrawal of 103 rejection for independent claim 57 and its dependent claims 72, 73, 80, 81, 85, and 93.

103(a) Rejections based on Drzaic, Roman, and Sturm

Claims 51-53, dependent from claim 38 were rejected over a combination of Drzaic Roman and Sturm references. These claims recite that depositing the semiconductor from solution includes printing. The Applicant submits that these claims are patentable for at least the reasons mentioned above for an independent claim 38. As mentioned, a combination of Drzaic and Roman fails to teach forming a patterned layer of semiconductor and does not make obvious depositing a patterned semiconductor (by, e.g., printing). Since Drzaic and Roman fail to teach depositing a pattern of semiconductor material, the Sturm reference, which describes printing, will not direct one skilled in the art to printing the semiconductor material in a pattern, as disclosed in claims 51-53. It is also important to note that Sturm, like Roman, is not concerned with using two-terminal switching devices in a pixel control circuit. Further, Sturm discloses only three-terminal (transistor) devices for switching. The Applicants, therefore, respectfully request withdrawal of 103 rejection for claims 51-53.

103(a) Rejections based on Drzaic, Roman, Sturm, Lamotte, Yamada, and Ohya.

Claim 55 dependent from claim 38 was rejected over a combination of Drzaic, Roman, and Lamotte. The Applicant submits that claim 55 is patentable in view of these references at least for the reasons discussed for the claim 38, from which it depends. The Lamotte reference does not provide any additional teaching that it may be advantageous to pattern a semiconductor layer in a two-terminal switching device. The Applicants, therefore, respectfully request withdrawal of 103 rejection for claim 55.

The independent claim 58 was also rejected over a combination of Drzaic, Roman, and Lamotte. The claim 58 has been amended to recite an operation of "forming a patterned semiconductor layer" The Applicants respectfully submit that claim 58 is patentable in view of these references for the reasons discussed for the claim 57. The Lamotte reference does not provide any additional teaching that it may be advantageous to pattern a semiconductor layer in a two-terminal switching device. The Applicants, therefore, respectfully request withdrawal of 103 rejection for claim 58, and for its dependent claims 59, 60, 64, 86, 87, 91, and 92.

Claims 65 and 66, dependent from claim 58 were rejected over a combination of Drzaic, Roman, Lamotte, and Sturm. Since Drzaic and Roman teach away from depositing a pattern of semiconductor material, and the Sturm reference, which describes printing, will not direct one skilled in the art to printing the semiconductor material in a pattern, as recited in claims 65-66. The Applicants, therefore, respectfully request withdrawal of 103 rejection for claims 65-66.

Claim 67, dependent from claim 58 was rejected over a combination of Drzaic, Roman, Lamotte, Sturm, and Ohya. Since Drzaic and Roman teach away from depositing a pattern of semiconductor material, the Sturm reference, which fails to overcome these deficiencies as described above, will not direct one skilled in the art to printing the semiconductor material in a pattern, as disclosed in claims 67. The Ohya reference does not provide any additional teaching suggesting that one should pattern the semiconductor layer in a two-terminal switching device. The Applicants, therefore, respectfully request withdrawal of 103 rejection for claim 67.

Claim 56 dependent from claim 38 was rejected over a combination of Drzaic, Roman, and Yamada. The Applicant submits that claim 56 is patentable in view of these references at least for the reasons discussed for the claim 38, from which it depends. The Yamada reference does not provide any additional teaching that it may be advantageous to pattern a semiconductor layer in a two-terminal switching device. The Applicants, therefore, respectfully request withdrawal of 103 rejection for claim 56.

Conclusion

In view of the above, Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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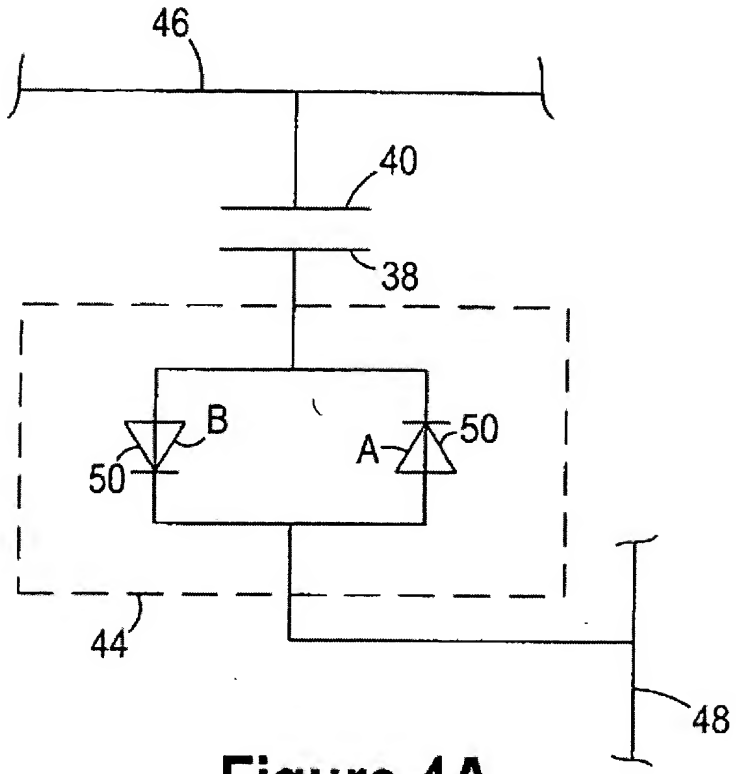

Figure 4A

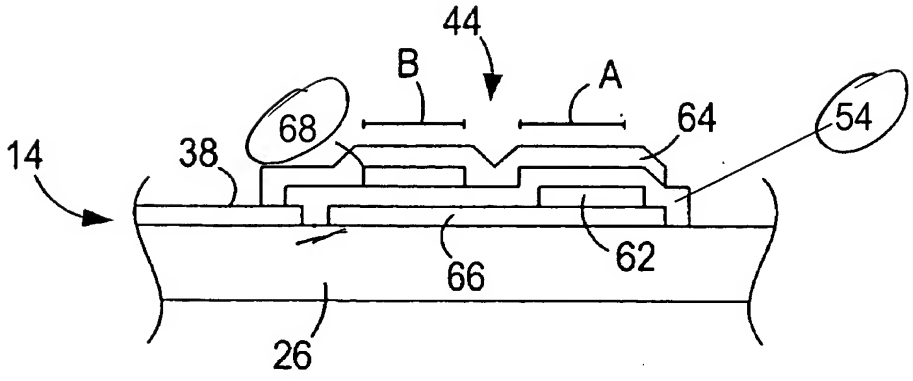

Figure 4B